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LAYOUT DESIGN OF A SYNAPTIC INPUT WITH DIGITALLY CONTROLLED WEIGHT COEFFICIENTS FOR A HARDWARE IMPLEMENTATION OF AN ARTIFICIAL SPIKING NEURON

Abstract. The layout design of a synaptic input with digitally controlled synaptic weight coefficients is presented as a building component of a spiking neuron hardware implementation. The design is based on Leaky Integrate-and-Fire model of an artificial spiking neuron. The compact-sized layout is obtained using EDA tool with all necessary physical verifications fulfilled at every design stage. Layout versus schematic check and the simulation of signal waveforms at ports are performed based on the extracted netlist to validate the design.
Keywords: spiking neuron, neuromorphic chip, synapse, synaptic weights, EDA tool, CMOS, VLSI.

Problem statement. Artificial intelligence systems are currently realized using computational algorithms of deep neural networks which are performed on CPU, GPU, and FPGA. But their hardware architectures cannot be optimized for massively parallel computations of such a level that allows us to simulate learning processes in the human brain. To execute massive AI algorithms using common hardware architectures we should spend enormous amount of memory, processing capacity, energy, and time. Increasing demands to the performance and efficiency of AI systems force us to design new architectural solutions for parallel computations typical for AI algorithms. The obvious solution is to go to neuromorphic computing which is directly inspired by processes in biological neural network of the human brain. Neuromorphic computer systems are best suited to perform massively parallel computing and provide the highest performance in AI applications. Neuromorphic chips, unlike conventional processors, do not emulate neural networks, but they are physically constructed as neural networks to mimic the neuro-biological architecture of the human brain. Each chip consists of thousands of interconnected simple computational elements, that functionally correspond to biological neurons. A hardware implementation of an artificial neuron can be based on the existing semiconductor

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technology, and the neuromorphic chip itself can be made in the form of very large-scale integrated circuit (VLSI) [1,2].

Analysis of recent research. Neuromorphic chips can be implemented using either analog or digital circuits. Digital circuit design is generally more simple but analog neuron implementation consumes less energy and requires less area on the silicon chip. There are many papers devoted to the hardware implementations of neurons and neuron networks [3-6]. A Leaky Integrate-and-Fire model of an analog neuron has been proposed in [7,8] to design a spiking neuron at the transistor (schematic) level and to build logic gates as simple neural networks. In [9] this model has been used for the transistor level design of the analog spiking neuron with digitally controlled weight coefficients. However, a layout design of the spiking neurons has not been fulfilled in the considered papers.

Objective of the paper. This paper focuses on a layout design of a synaptic input with digitally controlled weight coefficients for the analog implementation of a spiking neuron previously proposed in [9] and designed at the transistor level. The layout design is the most time, money, and skill consuming stage of IC design flow. Each layout design of an integrated circuit is a highly creative work that cannot be satisfactory automated using CAD tools and should be considered and protected as intellectual property (IP).

Main material presentation. An artificial neuron in terms of Leaky Integrate-and-Fire model consists of several building blocks shown in Fig. 1. The most significant blocks of the artificial neuron are synaptic inputs which produce weighted input signals. Like in a real neuron of the human brain, an input signal can be amplified or attenuated corresponding to synaptic weight coefficients. To this end excitatory and inhibitory weight input circuits are provided for each synaptic input. Post-synaptic signals from all synaptic inputs are added and formed post-synaptic potential of the neuron using a leaky integrator. The capacitor of the leaky integrator determines the level of the post-synaptic potential, and the resistive load ensures that the neuron returns to the relaxed state.

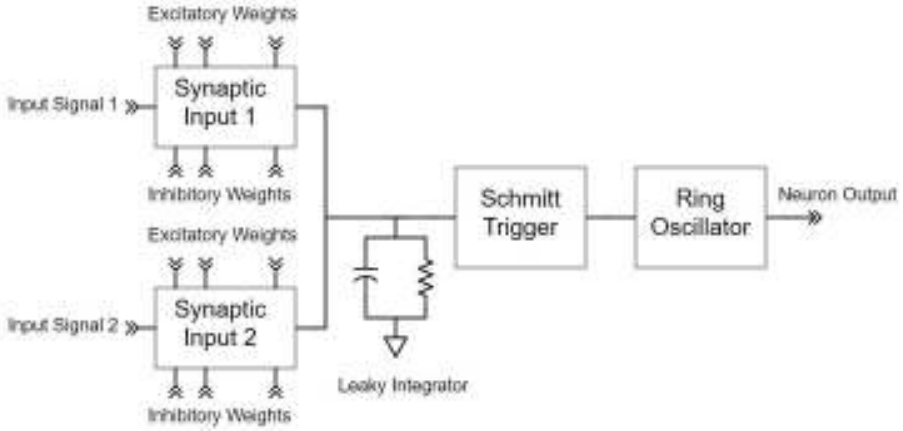

Figure 1 – Block diagram of an analog neuron with two synaptic inputs

A simple synapse realization relies on excitatory and inhibitory circuits consisted of several MOS transistors connected in parallel [7,8] as shown in Fig. 2. Voltages on the gates of these transistors regulate currents from the power source to the output and from the output to the ground. Interchanging only two voltages V_{base} and V_{offset}, where $V_{VDD} \geqslant V_{base} > V_{offset}$, on transistor gates in the subthreshold regime, we can obtain four variations of voltage level at the post-synaptic output node for three parallel connected MOS transistors in the excitatory circuit. In the same way four voltage levels are obtained for inhibitory circuit using $V_{GND} \leqslant V_{base} < V_{offset}$.

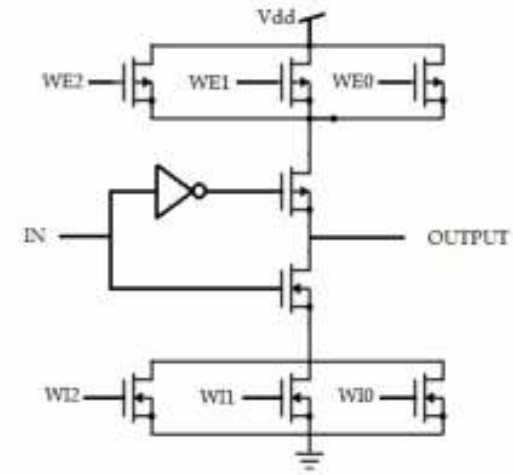

Figure 2 – Synaptic input circuit diagram [7]

To provide four voltage levels at the post-synaptic output node it is enough to use 2-bit numbers for digital weight control. Those numbers regulate the choice of one of two voltage levels applied to transistor gates acting as synaptic weight coefficients. In Fig. 3 it is shown the circuit diagram of a digital voltage control block with voltage switch blocks which provide digital control for voltage level applied to the gates [9].

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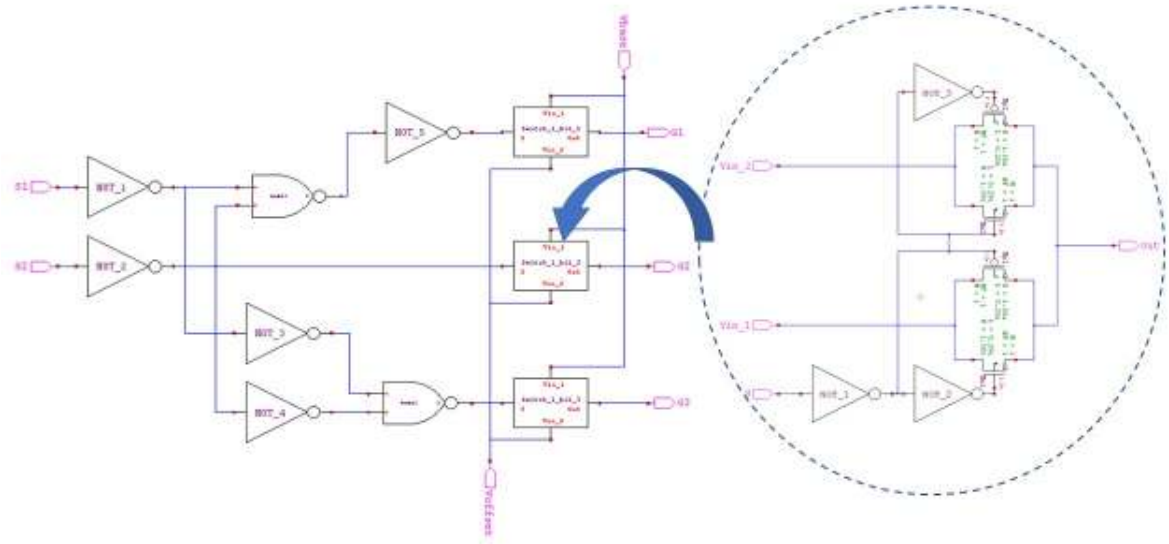

Figure 3 – Circuit diagram of a digital voltage control block

The most difficult stage of IC design flow is the layout or mask design which means the representation of an integrated circuit in terms of geometric shapes (polygons) which correspond to physical patterns of semiconductor, oxide, and metal layers required to prepare the integrated circuit for manufacture. Developing innovative layout designs is essential to produce small-sized, energy-effective digital devices.

Results of the layout design of the digital voltage control block is shown in Fig. 4. This block regulates voltages on the gates of three parallel connected MOS transistors in the excitatory or inhibitory circuit of a synaptic input.

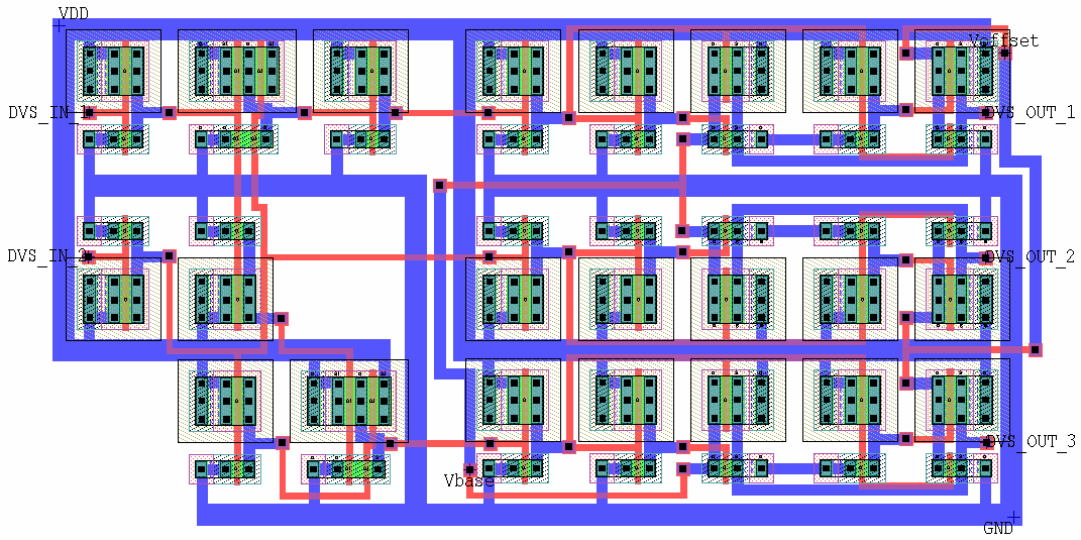

Figure 4 – Layout of the digital voltage control block

Combining this layout for excitatory and inhibitory circuit with the synaptic input circuit shown in Fig. 2 we can design the layout of a digitally controlled synaptic input. Then the topographies of two synaptic inputs are arranged and connected with each other and with power supply lines. The final layout design result for the synaptic input block is demonstrated in Fig. 5. This block weighs two pre-synaptic signals, add them and produce a post-synaptic potential of the neuron at the leaky integrator.

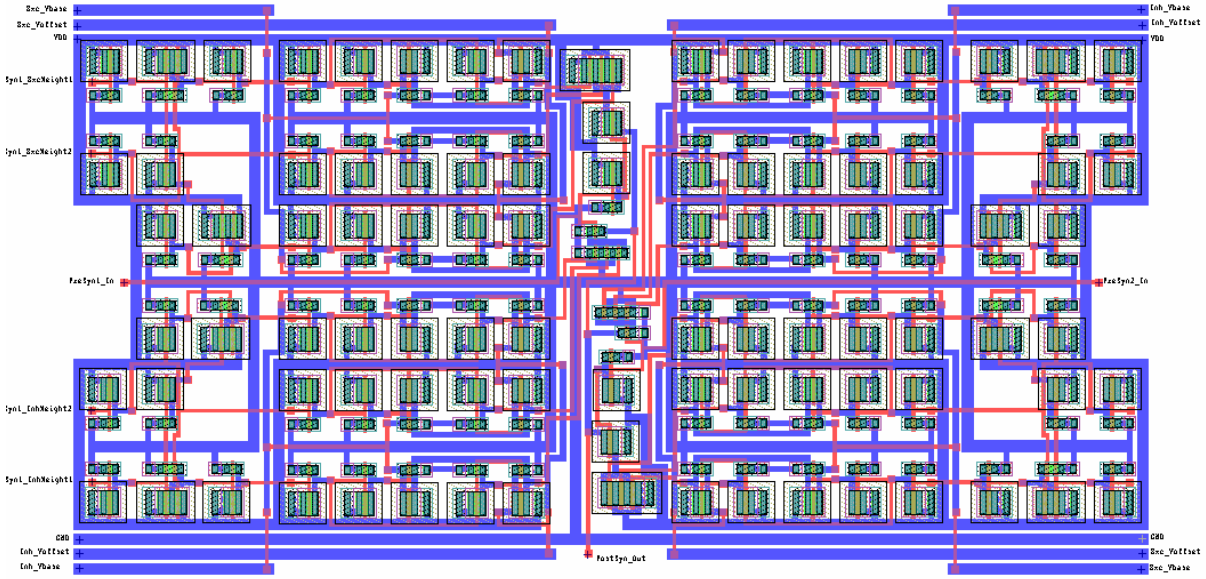

Figure 5 – Layout of the synaptic input block

At all stages of the design prosses physical verifications have been fulfilled in terms of design rule checking, electrical rule checking and parasitic extraction. The netlist has been extracted from the layout and layout versus schematic (LVS) check has been successfully performed. The netlist with the leaky integrator added has been used to obtain waveforms of signals at input and output ports and the results found a complete match with those demonstrated in [9] for the schematic level design.

Conclusions. The layout design of the digitally controlled synaptic input of an artificial neuron is carried out to reach as compact topography as possible fully satisfied to design rules accepted for a chosen technology level. Layout versus schematic check and all necessary physical verifications has been successfully performed. Waveforms of signals at ports have been simulated at every design stage and compared to those obtained at the schematic level to prove the correctness of the design.

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Проектування топографії синаптичного входу з цифровим керуванням ваговими коефіцієнтами для апаратної реалізації штучного імпульсного нейрона

Сучасні системи штучного інтелекту створюються з використанням обчислювальних алгоритмів глибоких нейронних мереж, що виконуються на центральних або графічних процесорах. Але такі апаратні засоби не оптимізовані для виконання паралельних обчислень за нейромережевими алгоритмами на рівні, достатньому для ефективного моделювання процесів навчання в людському мозку.

Рішенням цієї проблеми є перехід до нейроморфних обчислень, які безпосередньо надихаються процесами в біологічній нейронній мережі. Нейроморфний чіп, на відміну від звичайного процесора, складається з тисяч взаємопов'язаних простих обчислювальних елементів, які функціонально відповідають біологічним нейронам.

Метою роботи є проектування топографії синаптичного входу нейрона з цифровим керуванням ваговими коефіцієнтами, який є складовим елементом апаратної реалізації штучного імпульсного нейрона, спроектованого раніше на транзисторному рівні. При проектуванні використовувалась LIF (Leaky Integrate-and-Fire) модель штучного імпульсного нейрона. За допомогою системи автоматизованого проектування інтегральних схем створено компактну топографію синаптичного входу з використанням на кожному етапі проектування всіх належних методів фізичної верифікації. Для підтвердження достовірності проектування виконана перевірка відповідності топографічного та схематичного проектів на основі порівняння списків з'єднань та порівняння часових діаграм сигналів у портах.

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