UDC 004.272.43.003.13

V.P. Ivaschenko, G.G. Shvachych, E.V. Ivaschenko, V.V. Busygin

IMPROVING THE EFFICIENCY OF MULTIPROCESSOR SYSTEM THROUGH IN-LINE INTERFACE NETWORK AGGREGATION

This paper outlines ways to increase the efficiency of a multiprocessor system by changing the architecture of its network interface. It is established that the undoubted advantage of channels aggregation mode is a significant increase of data interchange between computing nodes of a multiprocessor system and a significant decrease in deceleration rate. The analytical ratios for the computations deceleration coefficient are derived. There was executed the stage of computations deceleration factor simulation and the regularity of its change depending on the applied computing platforms executed. It is shown that due to the mode of network interface channels aggregation, the multiprocessor system operation reliability increases. The current operating mode of the multiprocessor system network interface provides greater possibilities for implementation of data interchange procedure between the computing nodes, significantly improving the characteristics of its efficiency, performance and reliability of its operation.

Keywords: network interface, multiprocessor system, aggregation of channels, deceleration of computation, computing platform.transfer.

Introduction

Nowadays, there are many different options for building cluster computing systems. This paper considers so-called "blade" server solutions of multiprocessor systems [1,2]. However, one of the main differences in their design is in the network technology used, which selection is determined, first of all, by a class of problems that are solved by such systems.

For instance, in the metallurgy problems in mathematical simulation of long-length products thermal treatment, one of the main problems can be formulated as follows: there is a difference mesh of dimension M; the problem computation time in a single-processor system is determined by the t value. This parameter is not determinative. Here it is essential to increase the grid size, moreover, make it greater than the one that can be processed in a single processor memory. This procedure

is crucial for a more detailed computation of the corresponding processes, or for obtaining some new effects of the researched processes. In this regard, the issue of efficiency, performance and productivity focuses on the design of cluster systems. Thus, there considered the research problem of the network interface usage specifics in multiprocessor computing systems in solving tasks related to the computational area expansion. Thus, today, the theme of constructing clustered multiprocessor systems is relevant, interesting and experiencing the stage of its rapid development.

It is also clear that by high-performance clusters there was discovered an effective way of solving a wide range of topical problems. In our opinion, the new qualitative stage of multiprocessor cluster systems development is in the new modern network technologies. In this case, the efficiency of parallelizing computations depends on many factors, with the defining one that is the network interface organization selection. That is explained in such way. The cluster computing system network is fundamentally different from the workstations network, although for cluster construction requires ordinary network cards and hubs / switches that are used to organize the workstations network. However, in the case of a clustered computing system, there is one fundamental feature. The cluster network, ifirst of all, is not intended for computers communication, but for computational processes connection. In this respect, the higher the cluster network bandwidth, the faster the user-defined parallel problems on the cluster are solved. Thus, the computing network technical characteristics are of primary importance for multiprocessor cluster systems.

Until today, the problem of selecting and analyzing network technologies for modular multiprocessor cluster systems has not been properly developed. In addition, there are practically no papers devoted to the research of the network technologies impact on the parallelization efficiency in modular multiprocessor cluster systems. In this regard, the researches considered in this paper are relevant and of an interest kind to the relevant specialists.

Statement of the research problem, the research purpose and problems

The network interface operation modes analysis of a multiprocessor system allowed to reveal such a problem: how, due to the design fea-

tures of computer networks architecture in multiprocessor systems, can one achieve an increase in its efficiency and performance?

This problem can be solved by the fact that data interchange between computing nodes of a multiprocessor system can be referred to a separate network that works on the channel (second) level using channel bonding technology. This allows you to increase the speed of data exchange between the nodes of the system and reduce the download of the channel that connects them [3]. This network interface architecture implements high-speed node access memory. Generally, we note that the use of the reconfigurable network can improve the efficiency of the multiprocessor system, adapting the structure of its means to solve each specific type of task. Hence, the network architecture of a multiprocessor system should ensure, firstly, an increase in the speed of computing when solving tight tasks, and secondly, high-speed access to the memory of the nodes, reducing the download of the channel that connects them. In order to increase the bandwidth of the network system, it is recommended to apply the aggregation procedure or channel bonding technology. Such technology allows to combine several network adapters into one high-speed channel.

The purpose of the research is to provide the network interface channels aggregation mode in such a way that several computing networks that operate symmetrically, on the basis of the corresponding switching matrices, get configured in the data interchange network of the multiprocessor computer system.

At the same time it is necessary to solve the following problems:

1. Identify the basic rules regarding the problem computation time, depending on the change in the computing area of a multiprocessor system, based on the aggregation mode application of network interface channels.

2. Run the simulation stage of the basic time characteristics of the solved problem by applying a multiprocessor computing system, based on of the network interface channels aggregation. Identify the main regularities of the problem solution time depending on the computing area expansion.

3. Perform research aimed at determining the deceleration factor associated with the implementation of the network interface aggregation mode.

4. Run the simulation phase of deceleration computation and reveal conformity of its change, depending on the network interface channels number.

Presentation of the main research material

It is known [3] that multi-channel operation modes of a multiprocessor system computer network allow not only to improve the efficiency of parallelization, but also significantly reduce the computation time, as well as significantly accelerate them. Such results can be achieved by reducing the time boundary interchange between the computing nodes of the cluster system. At the first stage of the research, the main analytical relationships were drawn to determine the performance evaluation of a multiprocessor system.

So, let's consider the issue of determining the deceleration factor (K) associated with the computing area increase in the multiprocessor system, distributed over its nodes, compared with the version of the computer with an unlimited computing area. It is obvious that such a deceleration value is determined by the ratio of the form:

$$K = \frac{T_c^N}{T_c^1} \quad (1)$$

Here, T_c^N is the computation time of a single iteration with the use of N computing nodes, seconds, and T_c^1 is count time of a single iteration for a single-processor computing system. The ratio (1) shows that such a coefficient is determined taking into account the increase of the computing area, distributed over the nodes of the multiprocessor system. Then, when using a multiprocessor system, the total computation time of a single iteration is determined on the basis of the following ratio:

$$T_{\text{it}} = T_c^N + T_{ex}. \quad (2)$$

Under these conditions, T_{ex} is the boundary time of the data interchange between the cluster nodes, seconds. It should be noted that if the time of iteration computation only depends on the processor power, the time of the boundary data interchange is determined by grid size, number of cluster system nodes and the computer network bandwidth. Consequently, the value can be defined as follows:

$$T_{ex} = \frac{m \cdot N \cdot \sqrt{\frac{S}{\pi}}}{k \cdot d \cdot V_p} . \quad (3)$$

The value of m can be equal to one for unilateral mode of boundary data interchange or to two for two-way, Vp is the network interface port throughput (Gbit/s), N is the multiprocessor system nodes number, S is the total volume of the multiprocessor system computing area, k is the communication channels number of the computer networks working simultaneously (number of computing networks), d - half-duplex (d = 1) or duplex (d = 2) mode of the cluster system's computing network.

Taking into account the relation (2), we obtain:

$$K = \frac{T_c^N + T_{ex}}{T_c^1(S)} . \quad (4)$$

Taking into account the relation (3.4), the deceleration factor (K) value can be presented in an analytic-friendly form:

$$K = \frac{1}{N}(1 + \frac{T_{ex}}{T_c^N}). \quad (5)$$

For analyzing convenience of obtained results, the relation (5) is represented as:

$$K = \frac{1}{N}(1 + K_1). \quad (6)$$

In the relation (6), K1 is defined as:

$$K_1 = \frac{T_{ex}}{T_c^N} . \quad (7)$$

Such a coefficient can be interpreted as the calculations factor of the active deceleration. This is due to the fact that this value mainly affects the computation deceleration coefficient as a whole. Finally, based on the relations (5 - 7) there can be determined the multiprocessor system nodes number (Nid), which corresponds to the minimum computation deceleration. So, we have:

$$N_{id} = \sqrt[3]{\left(\frac{k \cdot d \cdot V_p \cdot \sqrt{\pi \cdot R}}{m \cdot V_c} \right)^2} . \quad (8)$$

In the relation (8) R represents the available node RAM of the multiprocessor system R (Gbits). In accordance with the above relations, computing experiments were carried out for a computer platform with

 ISSN 1562-9945

an Intel E8400 3 GHz processor. Here, as the initial ones, there were corresponding characteristics of the class of problems solved by a cluster system. These parameters are given in table 1

Table 1

Data for computing the system characteristics with an *Intel E*8400 3 *GHz* processor computer platform

V_p	10(8) Gbps
T_c^1	100 s
V_c	14 . 10 9 bit/s
R	24 Gbit
m	2
d	2
k	2

At the first stage, there was performed the simulation procedure of the time dependence of a single iteration calculation on the size of multiprocessor system computing area. The simulation results are presented as graphic dependencies (Fig. 1).

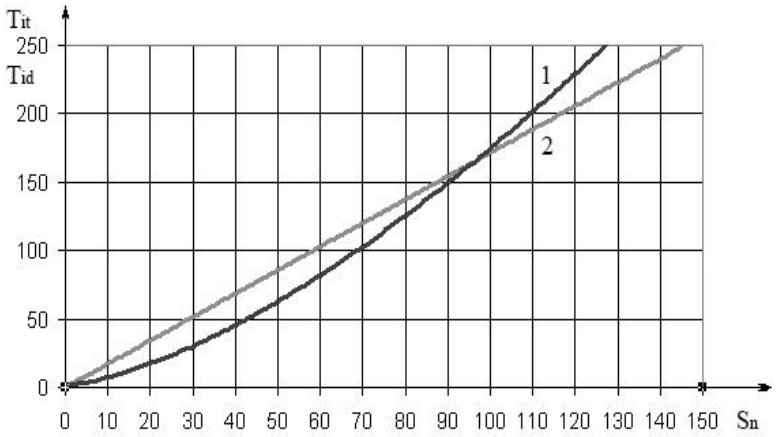

Figure 1 - The curves of the time dependence of a single iteration computation on the size of the multiprocessor system computing area for the of the network interface channels aggregation mode

It is quite obvious that the network aggregation mode allows the network equilibrium point to be substantially moved towards an increase in the computation area S_n. This becomes possible by increasing the speed of data interchange between the system nodes and reducing the channels download that connect them [4-6]. It is obvious that this network interface mode is implemented when $S_n < S_{id}$, and under such conditions the multiprocessor system computing time becomes less than the

time computed by ideal computer. This is due to the increase in processors number of the multiprocessor system.

At the second stage of the research, a procedure was performed to simulate the computations deceleration rate, depending on the nodes number of the multiprocessor system when the aggregation process of the network interface channel was implemented. The simulation results are presented as graphical dependencies (Fig. 2).

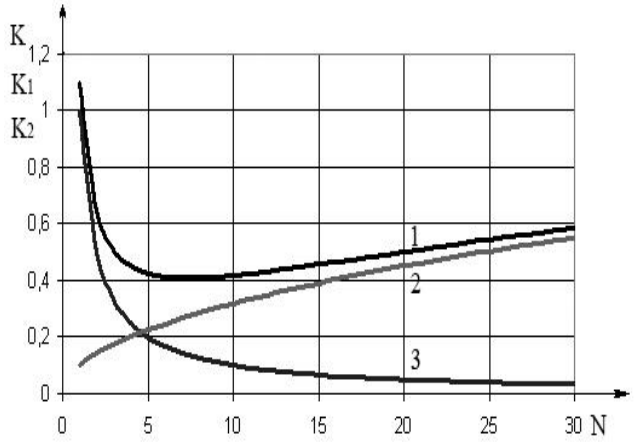

Figure 2 – The curves of the deceleration rate dependence on the multiprocessor system nodes number for the aggregation mode of the network interface channels

Figure 2 shows the general trend of decreasing the deceleration rate. Against the background of noted features, significant reduction in the time limit data interchange and the deceleration rate value. By means of the defined, we get that in this case $N_{id} = 5$, while the smallest computations deceleration value corresponds to $K = 0.4$.

The simulation specifics of the computations deceleration rate, depending on the number of network interface channels, are summarized in Table 2

Table 2

The simulation specifics of the computations deceleration rate, depending on the number of network interface channels

Number of network interface channels, k	*Optimal number of nodes in a multiprocessor system, N*	*The computation deceleration ratio, K*
1	*3*	*0.65*
2	*5*	*0.4*
4	*8*	*0.22*

 ISSN 1562-9945

The given data testify to the perspective of the research chosen direction. The proposed approach provides a uniform load distribution between the corresponding nodes in the multiprocessor system, and also helps to increase the data interchange speed between its nodes. Obviously, the higher the network bandwidth, the faster the parallel problems will be solved and the lower the deceleration rate will be.

Conclusions

1. This paper outlines ways to improve the multiprocessor system's efficiency by changing the network interface architecture. It is established that the undoubted advantage of the channels aggregation mode is in a significant increase in data interchange between computing nodes of a multiprocessor system, and a significant decrease in deceleration rate.

2. The main feature of the proposed network interface operation mode is that the reliability of the operation of the multiprocessor system increases. So, in the event of adapter failure, the traffic is sent to the next valid adapter without interrupting the computing process. If the adapter starts working again, the data transfer through it restores again.

3. The basic regularities regarding the problem computation time are revealed, depending on the calculations area change of the multiprocessor system in the network interface channels aggregation mode. It is shown that this approach allows to increase the system network interface bandwidth and significantly reduce the deceleration rate.

4. The current operating mode of the multiprocessor system network interface provides greater possibilities for implementation procedure for data interchange between computing nodes, significantly improving the characteristics of efficiency, performance and reliability of its operation.

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 ISSN 1562-9945