A.S. Tonkoshkur, A.V. Ivanchenko

ALGORITHM FOR SOFTWARE IMPLEMENTATION OF DESIGNING OVERVOLTAGE PROTECTION IN PHOTOVOLTAIC MODULES OF SOLAR ARRAYS USING A VARISTOR-POSISTOR STRUCTURE

Abstract. The use of modern hardware and software design allows to effectively solve a number of problems associated with the development of various technical devices. The specificity of this approach is the development of algorithms with the capabilities of dynamic correction of the design process with the participation of the user. The algorithm of the software implementation of designing protection circuits against electrical overloads in photovoltaic modules of solar arrays using a voltage limiting device based on metal oxide varistor and posistor of the PolySwitch type being in thermal contact is described in this paper. The algorithm provides for determining the optimal technical parameters of the voltage limiting device (minimum resistance and tripping current of the posistor element, classification voltage and non-linearity coefficient of the varistor element) for the operation of photovoltaic module, which is in the state of lighting in the absence and presence of faulty, degraded, or shaded photovoltaic cells.

Keywords: algorithm, design, approximation, modeling, photovoltaic module, overvoltage protection.

Introduction. Currently, solar arrays are one of the most popular renewable sources of electrical energy. The actual task in their further development is directly related to improving the reliability of their operation and service life.

One of the factors of unreliability of the solar battery is the presence of overvoltages inside its photovoltaic (PV) modules, which lead to the appearance of local heating regions ("hot spots") [1-3].

The PV module (solar panel) consists of series-connected PV cells that are divided into several submodules [4, 5]. Each such submodule is equipped with a bypass diode, which is connected in parallel to it. If one or more PV cells reduces the photocurrent generated by them due to a malfunction or shadowing (such PV cells are called "bad"), then the bypass diode D provides

an alternative current path from other submodules. The voltage across the entire submodule coincides with the low voltage drop across the directly biased diode (less than 1 V) [6]), which corresponds to an almost short circuit of the considered submodule.

The lighted cells inside the submodule cannot transfer their generated photocurrents to the external electrical circuit, because the series connection contains a big resistance created by the "bad" cells. The voltage created by these PV cells shifts the p-n junction of the "bad" element in the reverse direction, and it operates as a load, and not as a generator. Energy dissipation on the indicated load leads to inhomogeneous heating of the module, in particular, to the appearance of local heating regions in it. The number of PV cells in the submodule must be small in order to prevent the voltage on the "bad" cell U_R from exceeding the breakdown voltage of its reverse biased p-n junction U_b. If this is not done, then the PV cell will be heat up. High temperatures in local areas of PV cell can lead to the appearance of "hot spots". Thus, thermal breakdown of the p-n junction can occur as the cell temperature increases. In this case, the magnitude of the reverse voltage decreases, but does not increase with increasing current, and local thermal drift in time takes place. In this one-dimensional current channels are formed, which can lead to internal temperatures significantly exceeding 400 °C and damage to the PV cell [2]. "Hot spots" with or without thermal breakdown can lead to degradation and destruction of PV cells.

Problem statement. Among the circuitry means for protecting PV cells from overvoltages, one of the new approaches to the problem of protection against overvoltages of this type is the use of voltage limiting devices based on a varistor-posistor structure [7]. For its perspective implementation, it is necessary to justify and develop general schemes for using the solid-state structure under consideration to limit the constant overvoltages that occur in PV systems of solar arrays, as well as determine the requirements for their parameters. The most effective solution to this problem can be made using modern hardware and software design. Moreover, the specifics of applying the approach to the design of these systems is the development of algorithms with

the possibilities of dynamic correction of the design process with the participation of the user.

The algorithm of this kind for the software implementation of designing protection circuits against electrical overloads in PV modules of solar arrays using a varistor-posistor voltage limiting device based on metal oxide varistor and resettable fuse of the PolySwitch type being in thermal contact is described in this paper.

Main part.

1. Circuit representation of the implementation of overvoltage protection. As know, the implementation of overvoltage protection of an element of an electric circuit is realized by installing the corresponding voltage limiting device parallel to it [8, 9]. This approach makes it possible to propose an electrical circuit for the protection of one or series connected PV cells from overvoltages in the submodule of PV module (Fig. 1).
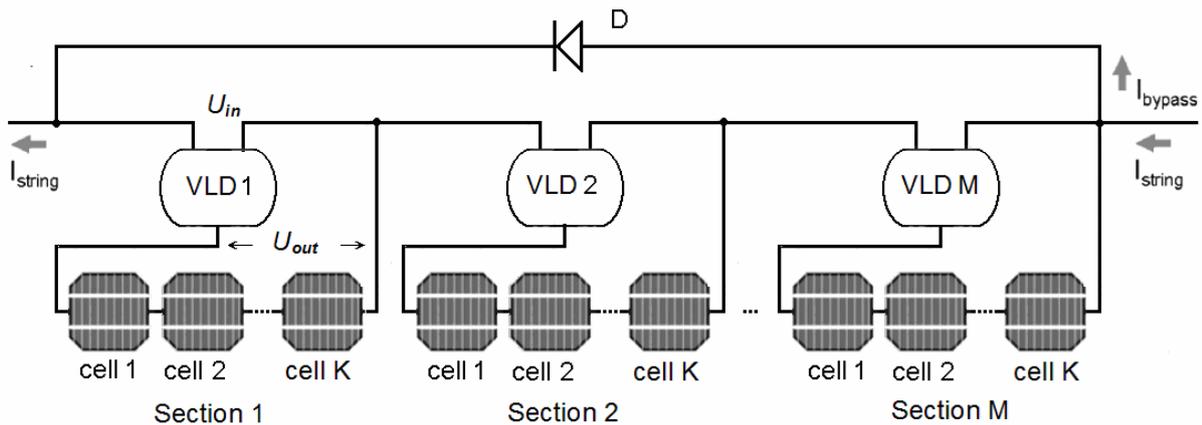
Figure 1 – Scheme of inclusion of voltage limiting devices for protection PV cells. *VLD* 1, *VLD* 2 … *VLD* M are the voltage limiting devices. U_{in} and U_{out} are the input and output voltage of the voltage limiting devices; D is the bypass diode; K is the number of PV cells in the section of the PV module; M is the number of sections in the PV submodule; I_{string} and I_{bypass} are the current coming from other submodules and the current through the bypass diode ($I_{bypass} \approx I_{string}$)

Several series-connected PV cells are connected to the output circuit of a separate voltage limiting device. The serial connection of the input cir-

cuits of the indicated voltage limiting devices and the bypass diode connected in parallel to them form a submodule of PV module.

The combined two-layer structure is used as the voltage limiting devices [10, 11]. One layer of this structure is varistor ceramics. The second layer is nanocomposite used in PPTC (polymeric positive temperature coefficient) fuse of the PolySwitch technology. These layers are in thermal contact. The equivalent circuit of such combined structure and its transient characteristic are shown in Fig. 2.
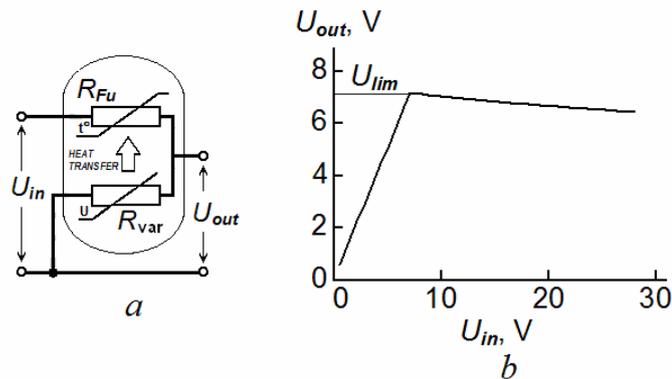
Figure 2 – Equivalent electrical circuit (a) and transient characteristic $U_{out}=f(U_{in})$ of voltage limiting device based on varistor-posistor structure

Thus, the resettable fuse is switched on between the separate sections of the PV cells, and the varistor is switched on in parallel to each section. When an input overvoltage is applied to such a structure, the current flowing through the varistor layer heats it. The heat dissipated by this varistor layer heats the posistor layer connected in series to it and leads to an increase in the resistance of this posistor layer. As a result, there is a redistribution of the input overvoltage between the layers. This ensures voltage limitation at a given value on the varistor layer (output voltage) and, therefore, on the load, which is connected in parallel with the varistor layer.

The project algorithm takes into account that PV cells have nonlinear current-voltage characteristics that depend on the level of solar radiation, ambient temperature and the features of the cell itself. Currently, there are several basic substitution schemes for PV cells, whose mathematical description is used in modern simulation [12-14].

The most well-known of them contains a photocurrent source (i_{ph}) and a parallel-connected diode (D) simulating a p-n junction, shunt resistor (r_{sh})

simulating leakage currents, and series resistor (r_s), which characterizes internal resistance of the cell and contacts (Fig. 3). r_L is the load resistance for PV cell.
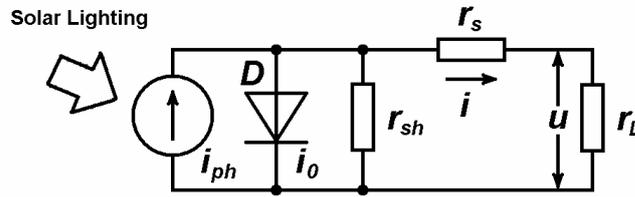
Figure 3 – Equivalent substitution scheme for PV cell

In the operating mode of the PV cell (directly biased photodiode) the leakage current is neglected, i.e. it is assumed that shunt resistance r_{sh} tends to infinity. In accordance with this substitution schemes, the output current of the PV cells i can be determined [12, 13] from the equation

$$i = i_{ph} - i_0 \left\{ \exp\left[\frac{q \cdot (u + i \cdot r_s)}{A \cdot k \cdot T} \right] - 1 \right\},$$ (1)

where A is the coefficient depending on the physical properties of materials and the p-n junction parameters (for silicon, it is assumed to be 1.2 - 1.8 [12, 15]); k is the Boltzmann constant; T is the absolute temperature of the PV cell; q is the electron charge; u is the output voltage of the PV cell; i_0 is the reverse current of the p-n junction diode.

In addition to the indicated physical parameters of the PV cells, the technical parameters are also used: $i_{SC} = i(u=0) = i_{ph}$ is the short-circuit current of the PV cell (maximum current generated by the PV cell when its contacts are closed); $u_{oc} = u(i=0) = (AkT/q) \ln[(i_{ph}+i_0)/i_0]$ is the open circuit voltage of the PV cell (voltage drop at the p-n junction), which is created by the photocurrent i_{ph} if the current in the external circuit i is zero.

The following parameters of the PV cell and its equivalent circuit are used as the main (basic) initial values in the considered algorithm: short circuit current (i_{sc}), open circuit voltage (u_{oc}), series resistance (r_s), shunt resistance (r_{sh}) and breakdown voltage at reverse bias (U_b).

These parameters of the substitution scheme can be found from the current-voltage characteristics of PV cell [15, 16, 17].

The values determining during the design are the parameters of the varistor-posistor voltage limiting device: current in the conducting state (I_{Fu}), electrical resistance in the conducting state (R_{Fu}), temperature (T_{trip}), tripping current (transition current to the insulating state) at a temperature of 25°C (I_{trip}) of the resettable fuse element as well as the classification voltage (U_C), non-linearity coefficient β, electrical resistance in the initial (at voltage less than U_C) state (R_U) of the varistor element.

2. Models describing the operation of the photovoltaic submodule

2.1. Submodule does not contain "bad" photovoltaic cells. All PV cells are forward biased and have low resistance when the entire submodule is lightened and all its PV cells are identical. Current Istring=Isubpanel flows through the submodule, and the bypass diode D is off (Fig. 1). In this state, the presence of the voltage limiting device does not affect the operation of the submodule, i.e. this voltage limiting device is in a conducting state (Fig. 4a).
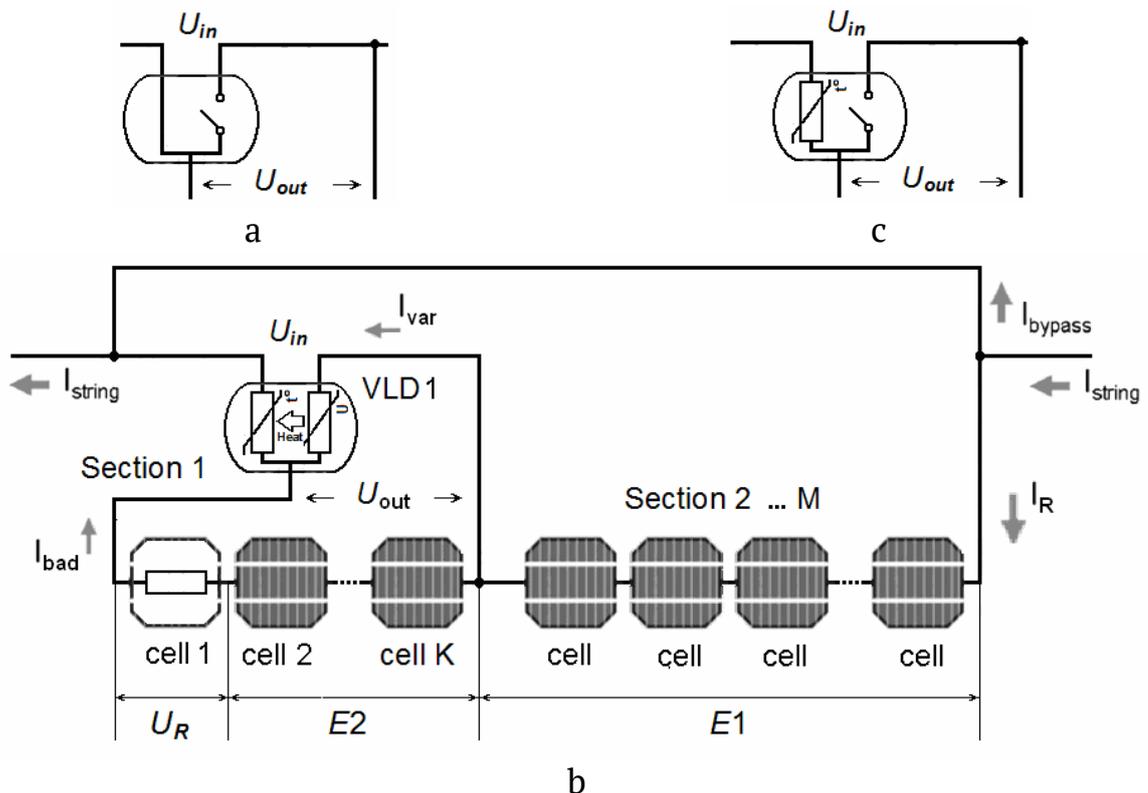
Figure 4 – Equivalent circuits illustrating the state of *VLD* 1 in the absence of "bad" PV cells (a), in the presence of one "bad" PV cell (b) and at the initial moment of relaxation after the renewal of the state of lighting of the PV cell which was in a state of shading (c). *Cell* 1 in *Section* 1 is the "bad" PV cell (has a reduced photocurrent). U_{lim} is the output voltage of the voltage limiting device;

I_R, I_{var}, and I_{bad} are the currents flowing through the PV cells of the submodule, the varistor element of the voltage limiting device and the shunt resistance of the "bad" PV cell

The following conditions must be met when realizing such a state of the voltage limiting device.

- The voltage generated by a separate section of the PV cells $K \cdot U_F$ (U_F is the voltage generated by the forward biased p-n junction of the lighted PV cell; K is the number of PV cells in a separate section of the PV submodule) and applied to the varistor must be less than the classification voltage of the varistor U_C (which must be less than the breakdown voltage of the reverse biased p-n junction of the section of the PV cells U_b)

$$K \cdot U_F << U_C < U_b. \tag{2}$$

The varistor must be in a state with high resistance, and thus it does not affect the operation of the PV cells.

- The resistance of the PPTC fuse in the conductive state R_{Fu} (determined by the passport values: the minimum initial resistance R_{min} or the maximum resistance after one hour after tripping at a given ambient temperature $R1_{max}$ [18, 19]) must be many times less than the equivalent series resistance of the PV cells section $K \cdot r_s$

$$R_{Fu} << K \cdot r_s. \tag{3}$$

- The tripping current I_{trip}, i.e. the minimum current flowing through the PPTC fuse at which the transition from a conducting to a non-conducting state occurs must be greater than the short circuit current of an separate PV cell ($I_{sc} \geq I_{string} = I_{subpanel}$)

$$I_{sc} \geq I_{trip}. \tag{4}$$

Upon meeting the conditions (2)-(4), the calculation of the light current-voltage characteristic $I(U)$ and the volt-watt characteristic $P(U)=I(U) \times U$ of the submodule can be carried out using well-known equations [12, 15, 20-21]

$$I = I_{SC} \cdot \left[1 - \exp\left[\frac{V - V_{OC} + I \cdot R_S}{U_T} \right] \right], \tag{5}$$

where $I_{SC} = i_{SC}$ is the short-circuit current of the PV submodule; $U_T = \left(A \cdot k \cdot T / q \right) \cdot n$ is the equivalent thermal voltage of the submodule;

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$U_{OC} = n \cdot u_{OC}$ is the open-circuit voltage of the submodule; $R_S = r_S \cdot K$ is the equivalent series resistance of the submodule; $n = K \cdot M$ is the number of PV cells in the submodule.

The characteristics of typical photoelectric submodule obtained in accordance with (5) are shown in Fig. 5.
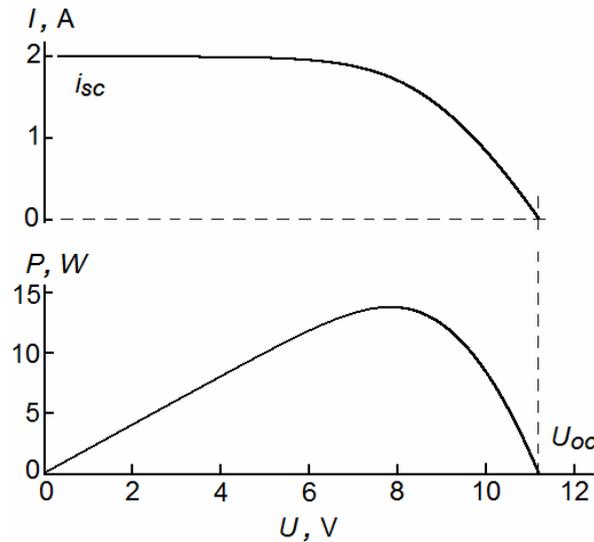
Figure 5 – Light current-voltage and volt-watt characteristics of the
PV submodule consisting of $n=20$ single crystal silicon PV cells

The parameters of the PV cells and its equivalent circuit used as the initial parameters of the considered algorithm are given in Table 1.

Table 1

PV cells parameters used in simulation

Parameters	Values
Short circuit current i_{sc}, A/cm^2	2
Open circuit voltage u_{oc}, V	0.56
Series resistance r_s, Ohm	0.05
Shunt resistance r_{sh}, Ohm	1000
Breakdown voltage under reverse bias U_b, V	12

2.2. Submodule contains "bad" PV cells. If in the section one (or several) PV cell is "bad", i.e. it has a reduced generation current, then the section resistance increases. The reasons for the appearance of "bad" PV cells may be their degradation, shading or malfunction. The current I_{string} begins to

flow through the bypass diode D (diode is on), which short-circuits the sub-module (Fig. 1 and 4b). As a result, a situation is realized when all the generated voltage by the lighted PV cells will be shift the "bad" PV cell (or cells) in the reverse direction. If the voltage of the voltage limiting device U_{lim} is less than the total voltage generated by the lighted sections of the PV cells located outside the *Section* 1 with a "bad" PV cell $E1 = K \cdot (M-1) \cdot U_F$ (Fig. 4b), i.e.

$$U_{lim} < E1, \tag{6}$$

then the varistor will be heat up transferring heat to the fuse. With increasing voltage limiting device temperature to T_{trip}, the fuse will be increase its resistance. As a result, the generated voltage $E1$ will be redistributed so that part of it will be drop on the high resistance of the PPTC fuse of the voltage limiting device, and the rest of the voltage (no more than U_{lim}) will be drop on *Section* 1.

In the presence of "bad" PV cells, the total shunt resistance of the "bad" PV cells, which is quite large (up to 10^4 Ohm [15]), is the load resistance of all series-connected lighted PV cells of the submodule. Thus, the following conditions hold:

$$i_{SC} \gg I_R; \quad U_F \approx U_{OC}. \tag{7}$$

The equations for determining the magnitude of the voltage drop on the "bad" PV cells of the submodule in accordance with Fig. 4b and approximations (7) are based on the use of Kirchhoff's laws and the heat balance equation:

$$\begin{cases} I_R = I_{\text{var}} + I_{bad}; \\ E1 = I_R \cdot [R_{Fu}(T) + r_s \cdot K \cdot (M-1)] + U_{out}; \\ I_{bad} \cdot [k_{bad} \cdot r_{sh} + r_s \cdot (K - k_{bad})] = U_R \cdot [k_{bad} + r_s/r_{sh} \cdot (K - k_{bad})] = U_{out} + E2; \end{cases} \tag{8}$$

where $U_R = I_{bad} \cdot r_{sh}$; $U_{out} = U_{out}(U_R) = U_R \cdot [k_{bad} + r_s/r_{sh} \cdot (K - k_{bad})] - E2$ is the output voltage of voltage limiting device (the voltage on the varistor element $U_{out} = U_{var}$); $E2 = (K - k_{bad}) \cdot U_F$ is the total voltage generated by the PV cells of the *Section* 1, except for the "bad" PV cells; k_{bad} is the number of "bad" PV cells; T is the temperature of voltage limiting device.

The system (8) can be transformed to the nonlinear equation with unknown U_R and T:

$$\left[\frac{U_R}{r_{sh}} + I_{var}(U_{out})\right] \cdot R_{Fu}^*(T) + U_{out} - E1 = 0,\qquad(9)$$

where $R_{Fu}^*(T) = R_{Fu}(T) + r_s \cdot K \cdot (M-1)$.

The equation for the heat balance of voltage limiting device, which also depends on these unknowns, can be written as follows

$$P_{var}(U_R) + P_{PPTC}(U_R, T) - \frac{T - T_0}{RT} = 0,\qquad(10)$$

where RT is the thermal resistance of the structure; $P_{var}(U_R) = I_{var}(U_{out}) \cdot U_{out}$

and $P_{PPTC}(U_R, T) = \left[\frac{U_R}{r_{sh}} + I_{var}(U_{out})\right]^2 \cdot R_{Fu}(T)$ are the electric powers dissipated by varistor and posistor elements respectively.

The main characteristics of voltage limiting device are presented in Fig. 6. The dependences of the output voltage of voltage limiting device U_{out}, which is applied directly to the "bad" PV cells, and the varistor current of voltage limiting device on the input voltage $E1$ for the situation under consideration (Fig. 4b), correspond to the case when the submodule contains one "bad" PV cell ($k_{bad}=1$). It is accepted that the voltage limiting device is used for individual protection against overvoltages of PV cell ($K=1$).

The main parameters that can vary are the electrical resistance of the posistor in the low-conductivity state R_{Fu0} and the thermal resistance of voltage limiting device RT.

As can be seen from Fig. 6a, a decrease in the thermal resistance of voltage limiting device (RT) slightly increases the voltage of limiting U_{lim}. Voltage limiting devices with smaller RT require higher currents of the varistor element necessary for heating and transition of the posistor element to a low-conductive state, which can not always be ensured by the characteristics of submodule. For example, if the voltage limiting device has $RT= 5$ K/W, then $I_{var}>2.5$ A is required to realize its tripping. Thus, the PV submodule considered here with the maximum current $i_{sc}=2$ A/cm^2 (Table 1) can not tripping such voltage limiting device. This must be taken into account when designing the considered protection system of PV cells from overvoltage, i.e. the heating current of varistor element must be less than the short circuit current of the PV submodule.

$$I_{var} < I_{SC}. \tag{11}$$

A change in the electrical resistance of the posistor in a low-conductive state does not lead to a significant change in the characteristics under consideration within the studied ranges. There is only a slight increase in the maximum heating current of varistor with a decrease in the electrical resistance.

a   b
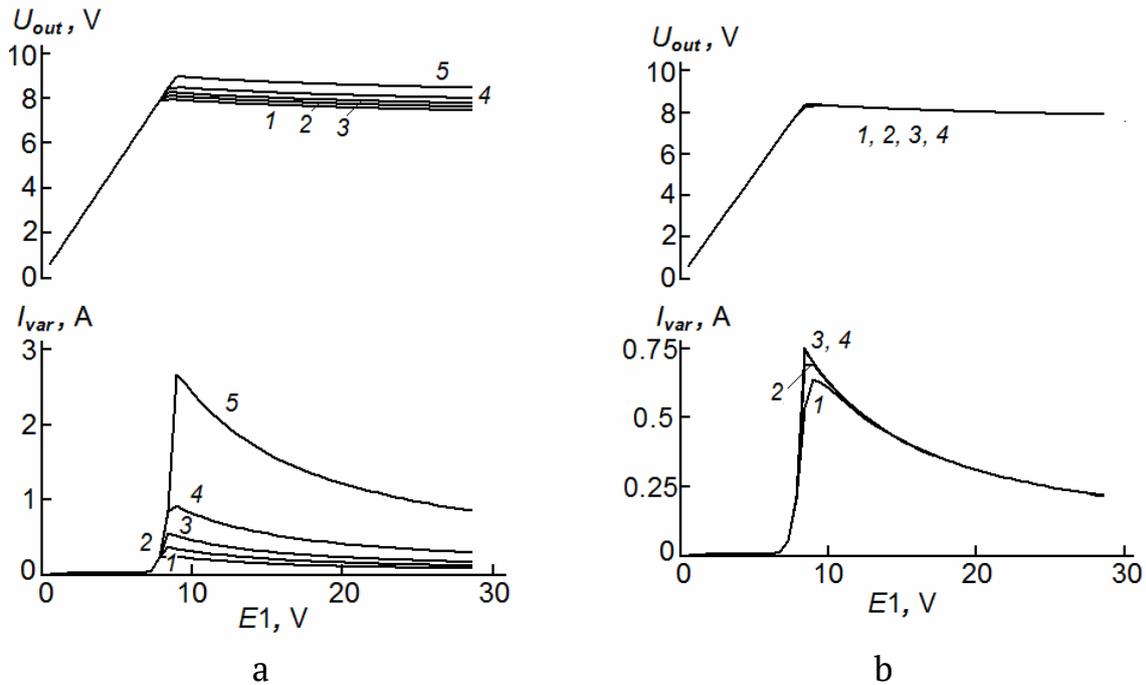
Figure 6 – Dependences of the voltage drop on the "bad" PV cell $U_R = U_{out}$ and the magnitude of the current flowing through the varistor layer of voltage limiting device I_{var} on the input voltage $E1$ for R_{Fu0}=0.001 Ohm; RT, K/Вт: $1 - 60$; $2 - 40$; $3 - 27$; $4 - 15$; $5 - 5$ (a) and RT=20 K/Вт; R_{Fu0}, Ohm: $1 - 0.1$; 2 -0.01; $3 - 0.001$; $4 - 0.0001$ (b)

It must be noted that if a section consists of several PV cells $K>1$ then the following restrictions must be fulfilled.

1. The voltage at a separate protected ("bad") PV cell must not exceed the breakdown voltage of its reverse biased p-n junction (Fig. 4b)

$$U_R = \left(U_{lim} + E2\right)/k_{bad} < U_b. \tag{12}$$

The influence of the resistance of directly biased lighted PV cells is not taken into account in (12), because $r_s/r_{sh} \ll 1$.

2. The voltage applied to the varistor element in the absence of "bad" PV cells must be less than its classification voltage, i.e. $E2 = K_{max} U_F < U_C$ (equation 2). K_{max} is the maximum possible number of series-connected PV cells in a section, i.e. $K_{max} = \max(K)$.

From these restrictions, the equation can be obtained for the maximum number of series-connected PV cells in the section

$$K_{\max} = \min[U_{\lim}/U_F, (U_b - U_{\lim})/U_F]. \tag{13}$$

The maximum number of PV cells in the section protected by one voltage limiting device can be obtained from the equation (13). Taking into account that the voltage generated by one PV cell is $U_F \approx 0.56$ V [15], the maximum number of PV cells in the section is 7, 10, and 7 when using varistor elements that provide the voltage of limiting U_{lim} equal to 4, 6 and 8 V, respectively. The highest voltage drop value on a "bad" PV cell occurs when it is alone in a circuit of series-connected lighted and serviceable PV cells.

2.3. Features of relaxation of voltage limiting device when renewing lighting of shaded PV cell. In accordance with the concepts [22], when returning submodule of the PV module from partially shaded in a fully lighted state the transition of the resettable fuse to a highly conductive ("cold") state can occur only when its temperature decreases due to a decrease in the supplied electric power. The initial stage of this process is illustrated in Fig. 1.

When the submodule of the PV module is fully lighted, the varistor resistance becomes large (shown by an open switch) due to the fact that a small voltage is applied to it. This voltage is generated by one section of the PV cells and it is less than the classification voltage of the varistor. The thermal power dissipated by the varistor becomes insufficient to maintain the resettable fuse at the tripping temperature. As a result, the temperature of the resettable fuse decreases and its resistance decreases. In the analyzed situation, condition (4) must be satisfied, i.e. the current through the voltage limiting device must be less than the value of the tripping current of the resettable fuse element I_{trip} at the actual temperature of the posistor layer.

The heat balance equation for the posistor layer, which describes such a process of relaxation of the voltage limiting device, can be written as:

$$C\frac{dT(t)}{dt} = P_{PPTC}[E,T(t)] - \frac{T(t)-T_0}{RT} \; ; \;\; T(t=0)=T_{trip}, \tag{14}$$

where $P_{PPTC}[E,T(t)] = \dfrac{R_{Fu}(T)}{R_{Fu}(T)+R_s}\dfrac{E}{R_{Fu}(T)+R_s}\cdot E$; $T=T(t)$; T_0 is the ambient temperature; t is the time; $R_{Fu}(T) = const / (T_{trip} - T)$ is the approximation of the temperature dependence of the PPTC fuse; $const = R_{Fu0}(T_{trip} - T_0)$ at $T_0 = 298$ K; $E = K \cdot M \cdot U_F$ is the electrical voltage generated by a PV submodule with voltage limiting device; C is the thermal capacity of voltage limiting device.

Typical relaxation dependences of the temperature of the voltage limiting device $T(t)$ and the electrical resistance of the posistor element of the voltage limiting device $R_{Fu}(t)$ are presented in Fig. 7. As can see, the previously mentioned parameters of the voltage limiting device also have a significant effect on these dependencies.
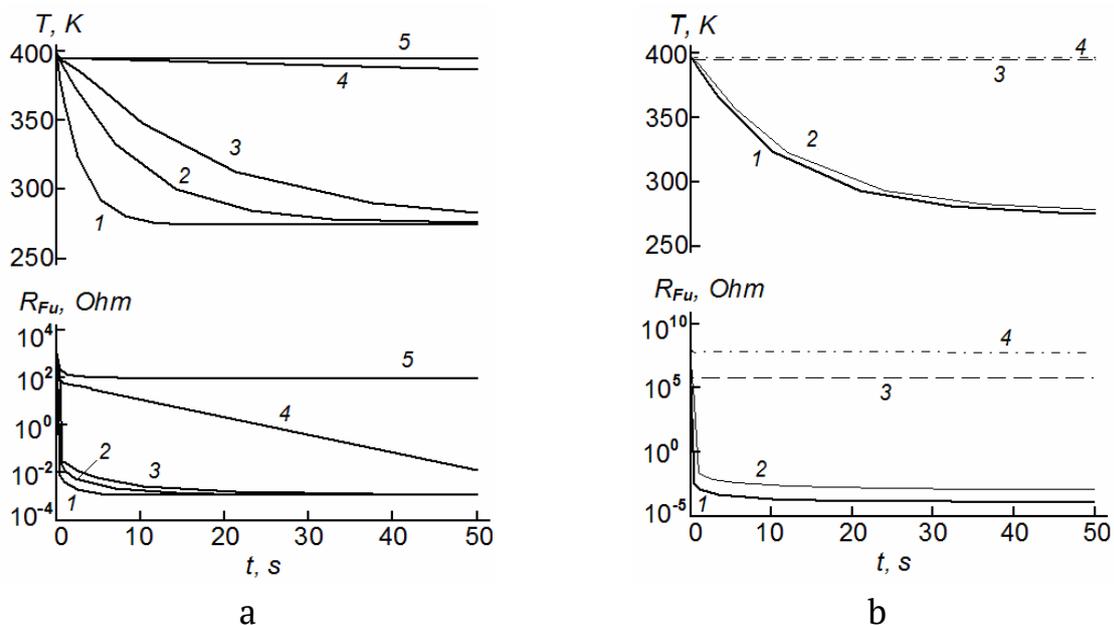
Figure 7 – Dependences of the temperature T and the electrical resistance of the PPTC fuse layer of the voltage limiting device R_{Fu} on the time t after resuming lighting of a previously shaded PV cell: when using the PPTC fuse with electrical resistance in the conducting state R_{Fu0}=0.001 Ohm and the voltage limiting device with thermal resistance RT, K/W: $1 - 5$; $2 - 15$; $3 - 27$; $4 - 40$; $5 - 60$ (a); when using the voltage limiting device with thermal resistance RT = 20 K/W and the PPTC fuse with electrical resistance in the conducting state R_{Fu0}, Ohm: $1 - 0.0001$; $2 - 0.001$; $3 - 0.01$; $4 - 0.1$ (b)

Relaxation of temperature and electrical resistance to their initial values (corresponding to the "cold" highly conductive state of the posistor) is possible only for voltage limiting devices that have small values of the thermal resistance of voltage limiting device RT (Fig. 7a, curves *1*, *2*, *3*) and the electrical resistance of posistor layer in conducting state R_{Fu0} (curves *1* and *2*). Relaxation is not observed at large values of indicated parameters.

3. Algorithm for determining the parameters of voltage limiting device for the submodule based on silicon photovoltaic cells. Based on the above results, the sequence for determining the optimal parameters of a varistor-posistor voltage limiting device can be represented by the following algorithm.

1. Determination of the parameters of the PV cells.

2. The choice of the voltage limiting device in accordance with conditions (2)-(4), (6) and (7) with the subsequent control of their implementation for all the above states of the PV submodule.

3. Simulation the operation of the PV submodule in the presence of "bad" PV cells. Clarification of the parameters of the voltage limiting device to ensure the required values of voltage of limiting (U_{lim}) and the heating current of the varistor (I_{var}) The operability test of the protection against the maximum possible overvoltages in the presence of only one "bad" PV cell $k_{bad}=1$.

4. Simulation the relaxation of the voltage limiting device when renewing lighting of shaded PV cell. Correction of such parameters of the voltage limiting device as the resistance of its varistor element in the conducting state R_{Fu0} and thermal resistance of the voltage limiting device RT in order to fulfill the required conditions for the implementation of relaxation.

Conclusions. The description of the design algorithm for a voltage limiting device based on metal oxide varistor and resettable fuse of the PolySwitch type being in thermal contact for protection against electrical overloads in PV modules of solar arrays is given in this paper.

The parameters of the PV cell and its equivalent circuit are used as the initial values in the considered algorithm: short circuit current (i_{sc}), open cir-

cuit voltage (u_{oc}), series resistance (r_s), shunt resistance (r_{sh}) and breakdown voltage at reverse bias (U_b).

Determination of the technical parameters of the voltage limiting device reduces to an analysis of the influence of their numerical values on the operation of the submodule of PV module, which is in the state of lighting in the absence and presence of faulty, degraded or shaded PV cells, as well as during relaxation to the lighted state of the shaded PV cells. Such technical parameters are the electrical resistance in the conductive state and the tripping current (current transition to the insulating state) at a temperature of 25 °C of the resettable fuse element; classification voltage, non-linearity coefficient β and electrical resistance in a low conductive state (at a voltage lower than the classification voltage) of the varistor element; total thermal resistance of the voltage limiting device.

The algorithm can be used to develop the software application for modeling systems protection against overvoltages of the considered type at the stages of selecting the element base and describing the functioning of the modern cycle of computer-aided design technology.

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Алгоритм программной реализации проектирования защиты
от перенапряжений в фотоэлектрических модулях солнечных батарей
с применением варисторно-позисторной структуры

Применение современного аппаратно-программного проектирования позволяет эффективно решать ряд задачь, связанных с разработкой различных технических устройств. Спецификой этого подхода заключается в разработке алгоритмов с возможностями динамической коррекции процесса проектирования с участием пользователя. В данной работе приводится описание алгоритма программной реализации проектирования схем защиты от электрических перегрузок в фотоэлектрических модулях солнечных батарей, которые используют ограничитель напряжения на основе металлоксидного варистора и позистора типа PolySwitch, находящихся в тепловом контакте. Алгоритм предусматривает определение оптимальных технических параметров ограничителя напряжения (минимальное сопротивление и ток срабатывания позисторного элемента, классификационное напряжение и коэффициент нелинейности варисторного элемента) для функционирования фотоэлектрического модуля, находящегося в состоянии освещения в отсутствии и при наличии неисправных, деградированных или затененных фотоэлектрических преобразователей.

Алгоритм програмної реалізації проектування захисту
від перенапруги у фотоелектричних модулях сонячних батарей
із застосуванням варисторно-позисторної структури

Застосування сучасного апаратно-програмного проектування дозволяє ефективно вирішувати ряд завдань, пов'язаних з розробкою різних технічних пристроїв. Специфіка цього підходу полягає в розробці алгоритмів з можливостями динамічної корекції процесу проектування за участю користувача. У даній роботі приводиться опис алгоритму про-

грамної реалізації проектування схем захисту від електричних перевантажень у фото-електричних модулях сонячних батарей, які використовують обмежувач напруги на основі металоксидного варистора та позистора типу PolySwitch, що перебувають у тепловому контакті. Алгоритм передбачає визначення оптимальних технічних параметрів обмежувача напруги (мінімальний опір та струм спрацьовування позисторного елемента, класифікаційна напруга та коефіцієнт нелінійності варисторного елемента) для функціонування фотоелектричного модулю, що перебуває в стані освітлення у відсутності та при наявності несправних, деградованих або затінених фотоелектричних перетворювачів.

Тонкошкур Александр Сергеевич - профессор, д.ф.-м.н., профессор кафедры ЭВМ Днепровского национального университета имени Олеся Гончара.

Иванченко Александр Владимирович - доцент, к.ф.-м.н., доцент кафедры радиоэлектроники Днепровского национального университета имени Олеся Гончара.

Тонкошкур Олександр Сергійович - професор, д.ф.-м.н., професор кафедри ЕОМ Дніпровського національного університету імені Олеся Гончара.

Іванченко Олександр Володимирович – доцент, к.ф.-м.н., доцент кафедри радіоелектроніки Дніпровського національного університету імені Олеся Гончара.

Tonkoshkur Alexander – professor, doctor of physical and mathematical sciences, professor at the Department of Electronic Computing Machinery of Oles Honchar Dnipro National University.

Ivanchenko Alexander– associate professor, candidate of physical and mathematical sciences, associate professor at the Department of Radio Electronics of Oles Honchar Dnipro National University.