DOI 10.34185/1562-9945-1-126-2020-05
UDC 004.315.2

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LAYOUT DESIGN OF 4-BIT RIPPLE CARRY ADDER BASED ON PASS TRANSISTOR LOGIC

Abstract. The full adder is a key element of any arithmetic logic units used in microprocessor systems. For microprocessor components created for modern mobile digital devices, compact layout design on the silicone chip is of great importance. In this paper an area effective layout design on the chip is proposed for 4-bit ripple carry adder based on pass transistor logic. The full adder is simulated using EDA tool and output signal waveforms are obtained to demonstrate the functionality of the design. It is shown that 1-bit full adder based on pass transistor logic and composed of two 3T XOR gates and one 2T multiplexer allows us to obtain area effective layout design on the chip for 4-bit ripple carry adder providing acceptable characteristics for output signals.

Keywords: silicon chip, layout, full adder, pass transistor logic, CMOS, EDA, VLSI.

Introduction. Arithmetic operations are considered as most important data conversions in digital signal processing systems. That is why the arithmetic logic unit (ALU) is the fundamental element of any microprocessor. The main building block of ALU is the full adder which realizes a set of basic arithmetic operations, such as addition, subtraction, multiplication and division. The performance for the whole computer system strictly depends on the efficiency of arithmetic operation executed by the full adder.

Increasing demands for portable computer systems such as cellular phones and laptops create serious challenges for designers in the area of very large scale integration (VLSI) systems. Low power consumption, high speed, small surface area on the silicon chip and high reliability become very important factors for combinational logic devices designed for VLSI circuits. Thus, a huge number of research projects are devoted to the design of VLSI circuit components based on different logic techniques to satisfy those contradictory requirements.

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SSN 1562-9945 (Print)
ISSN 2707-7977 (Online)

Conventional CMOS full adder design is based on complementary PMOS pull-up transistor and NMOS pull-down transistor networks [1,2]. The main advantages of conventional CMOS full adder are minimal power dissipation, full output swing, high noise margin and reliability especially at low voltages. However this design requires 28 transistors which occupy large area on the silicon chip and suffers from high consumption of power, weak output driving capability due to series connected transistors and large delay of signal propagation. That is why a large number of different designs have been constructed up to now for the full adder to strengthen advantages and reduce drawbacks.

The advanced full adder can be designed based on different types of logics. Gate Diffusion Input (GDI) logic [3] has PMOS and NMOS transistors connected to additional inputs instead of voltage source and ground which gives more flexible design and reduces power consumption. Transmission Gate (TG) logic [4] relies on connected in parallel PMOS and NMOS transistors to gates of which complementary signals are applied. This design makes it possible to reduce signal delay but remains high power consumption with weak driving capability. Complementary Pass Transistor Logic (CPL) [5] applies only NMOS transistors for logic operations with high mobility, but each signal is carried by two wires in complementary form. CPL design suffers from high threshold voltage drop for NMOS transistor design at low voltages. A modified version of CPL – Double Pass Transistor Logic (DPL) uses both PMOS and NMOS transistors for switching high and low logic signals with full output swing [6]. This allows us to reduce threshold voltage drop and power consumption. Pass Transistor Logic (PTL) family uses much fewer transistors then conventional CMOS logic, occupies less area on the chip, requires less power and runs faster.

For all types of logic there is the common aim to make a combinational device implementation on the chip as compact as possible. That is why the reduction in the number of transistors is critical for full adder designs based on any logic technique. But for really area effective full adder, a compact layout design on the silicone chip is of great importance. This paper is devoted to the

layout design of a compact 4-bit ripple carry adder which consists of 8T 1-bit full adders based on pass transistor logic.

Full Adder Schematic Design. The design is based on classical implementation of two XOR gates for sum output calculation and a multiplexer for carry output obtaining as shown in Fig. 1. Using pass transistor logic it is possible to reduce the number of transistors to eight. Fig. 2 demonstrates schematic level representations of 3T XOR gate and 2T multiplexer applied to the design.

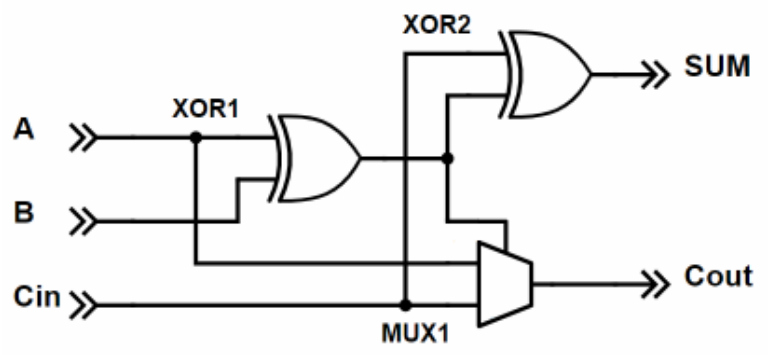
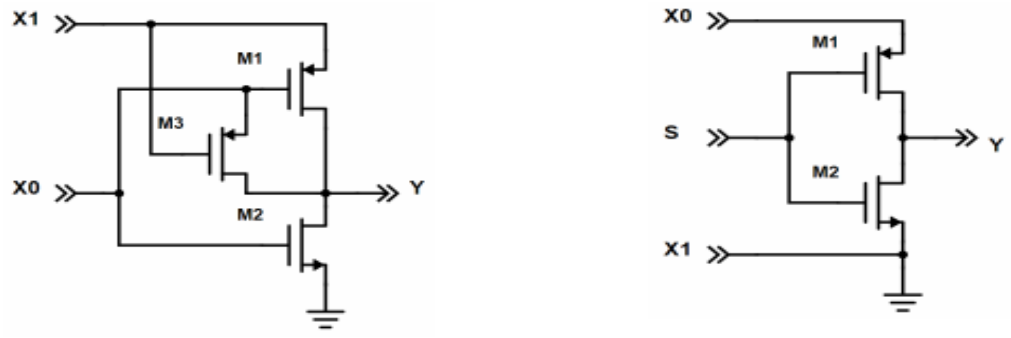


Figure 1 – Gate level of full adder design



a) b)

Figure 2 – Transistor representations for 3T XOR gate (a) and 2T multiplexer (b)

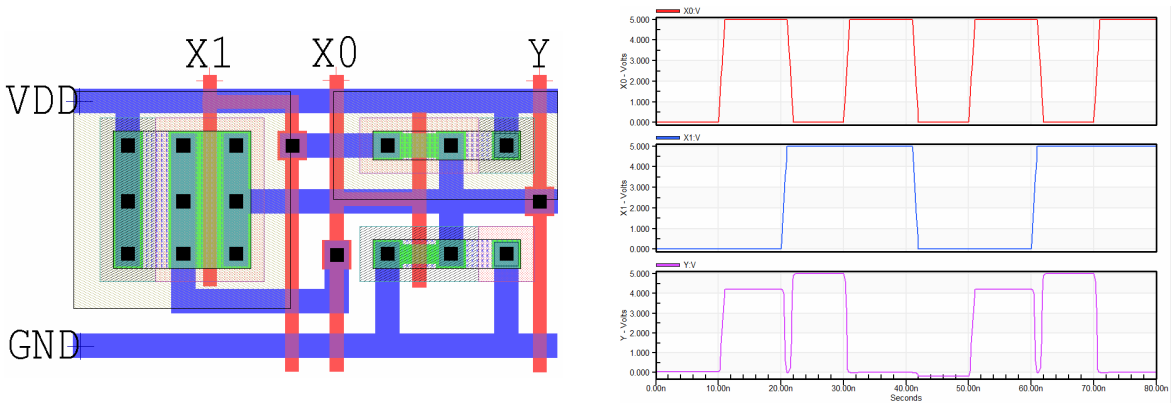
The reduction of transistor count for pass transistor logic should be paid by the voltage drop for output signals. Shown in Fig. 2(a) 3T XOR gate design is an inverter modified with PMOS pass transistor M3. With high logic level at input X1 this inverter works as a common CMOS inverter for the signal at X0 input. Low logic level at X1 leads the inverter to the state with high impedance. In such a case output Y should get the same logic value as at input X0 due to open PMOS pass transistor M3. But if at input X0 is high logic level while at input X1 is low logic level, some voltage degradation is observed at

SSN 1562-9945 (Print)
ISSN 2707-7977 (Online)

output Y due to threshold drop when signal passes transistor M3. To minimize the output voltage degradation, the W/L ratio of transistor M3 has to be increased and the same ratio of transistor M2 should be decreased. Similar voltage degradation problem occurs for the multiplexer shown in Fig. 2(b) when input X0 is fed by low logic level signal.

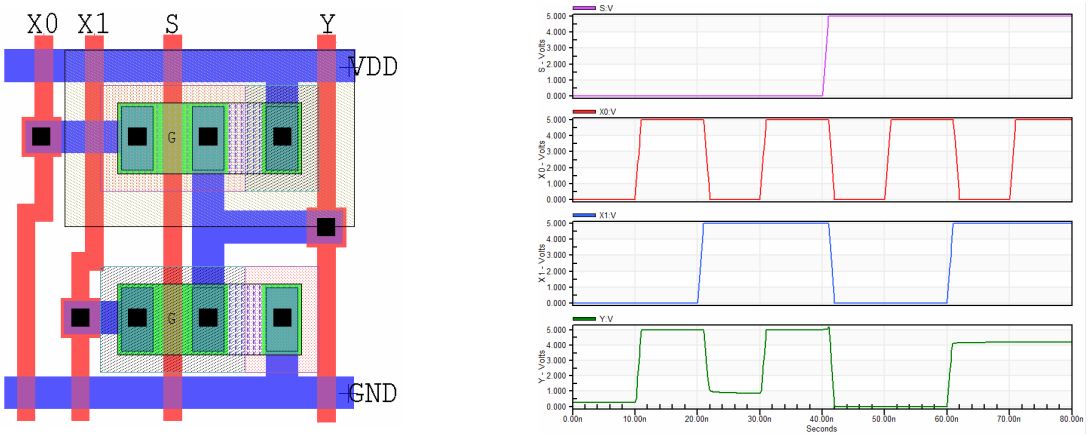
Full Adder Layout Design. The layout of 4-bit full adder is designed to obtain an area efficient topology on the silicone chip using an electronic computer-aided design tool. The schematic design of all full adder components has been performed to tune parameters of the transistors (W/L ratio). Then the layout design has been carried out to reach as compact topology as possible fully satisfied to design rules accepted for a chosen technology level. Layout versus schematic check (LVS) has also been performed. Waveforms of signals at ports have been simulated at every stage of the design.

The results of the layout design for 3T XOR gate and 2T multiplexer along with corresponding waveforms are demonstrated in Fig. 3 and Fig. 4. There is some voltage drop observed at waveforms of output signals when the high logic level signal runs across the pass transistor with the inverter network being in high impedance state.



a) b)

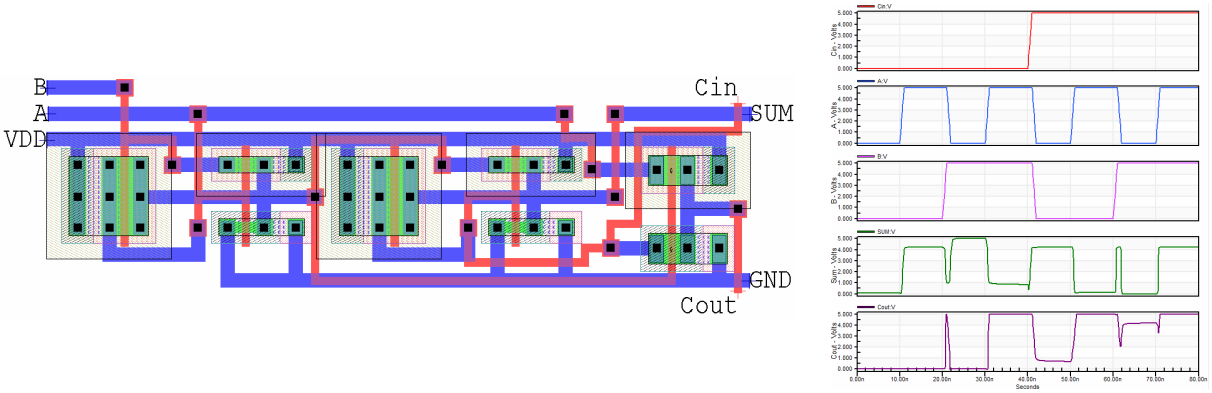
Figure 3 – XOR gate layout (a) and waveform view (b)



a) b)

Figure 4 – Multiplexer layout (a) and waveform view (b)

Fig. 5 demonstrates the results of the layout design and simulation for 1-bit full adder comprises two 3T XOR gates and one 2T multiplexer connected in correspondence with the logic level network shown in Fig. 1.

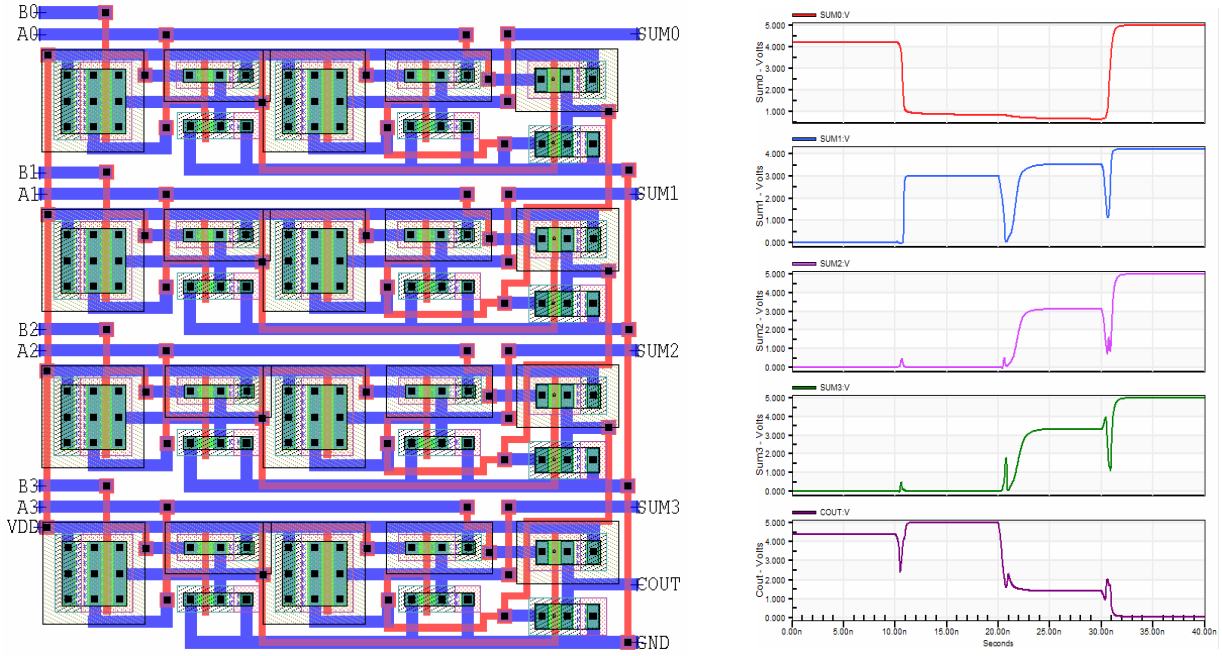


a) b)

Figure 5 – 1-bit full adder layout (a) and waveform view (b)

The layout design and simulation results for 4-bit ripple carry adder are shown in Fig. 6. The adder consists of four 1-bit full adders series connected through Cin and Cout outputs. A ripple carry adder produces a rather large delay of signal but due to very simple network organization it is advantageous for VLSI with compact topology. Fig. 6(a) demonstrates the area effective layout design with one layer of metallization. Total area occupied by 4-bit adder on the silicone chip has dimensions of 192x208λ.

SSN 1562-9945 (Print)
ISSN 2707-7977 (Online)



a) b)

Figure 6 – 4-bit full adder layout (a) and waveform view (b)

The simulation results of 4-bit adder are demonstrated in Fig. 6(b) for output ports only. The input ports are fed with the following bit sets:

A	0101	1011	0100	0010
B	1100	0111	1010	1101
Sum	0001	0010	1110	1111
Cout	1	1	0	0

As can be seen, there is some degradation of output logic signals due to pass transistor threshold problem. The high level logic signal decreases by the threshold voltage of the pass transistor and the low voltage level, on the contrary, increases when the signal goes through this transistor. To eliminate this problem, additional CMOS inverters can be inserted at output stages connecting the network to the sources and restoring logic level of signals. However, this improvement of the output waveforms must be paid by undesirable increasing signal propagation delay, power consumption and chip area occupied by the adder.

Conclusions. The pass transistor logic is now considered as a method to radically decrease the number of transistors involving into combinational device network. This results in decreasing power consumption, signal delay

and surface area on the chip. But for really area effective design of VLSI device, accurate and compact layout design of the device on the silicone chip is needed. This paper proposes a variant of compact layout design for 4-bit ripple carry adder using 32 transistors and one metallization layer for interconnects. The simulation results obtained as output signal waveforms demonstrate the functionality of the adder. This confirms the possibility of using the full adder designed in this paper as a key part of ALU for mobile devices.

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Received 13.01.2020.
Accepted 15.01.2020.

Топологічне проектування 4-бітного суматора з послідовним перенесенням на основі логіки на прохідних транзисторах

Повний суматор є ключовим елементом арифметико-логічних пристроїв, що використовуються у мікропроцесорних системах. Для компонентів мікропроцесорів, які призначаються для сучасних мобільних цифрових пристроїв, велике значення має щільність компоновки на кристалі кремнію. У даній статті пропонується компактна топологія для 4-бітного суматора з послідовним перенесенням на основі логіки на прохідних транзисторах. Повний суматор моделюється за допомогою інструментів автоматизованого проектування, з одержанням часових діаграм вихідних сигналів, що демонструють функ-

SSN 1562-9945 (Print)
ISSN 2707-7977 (Online)

ціональні можливості спроектованого пристрою. Показано, що використання логіки на прохідних транзисторах при проектуванні топології 1-бітного повного суматора, який складається з двох логічних елементів XOR на трьох транзисторах і одного мультиплексора на двох транзисторах, дозволяє одержати компактний 4-бітний суматор з послідовним перенесенням і забезпечити прийнятні характеристики вихідних сигналів.

Топологическое проектирование 4-битного сумматора с последовательным переносом на основе логики на проходных транзисторах

Полный сумматор является ключевым элементом арифметико-логических устройств, используемых в микропроцессорных системах. Для компонентов микропроцессоров, предназначенных для современных мобильных цифровых устройств, большое значение имеет плотность компоновки на кристалле кремния. В данной статье предлагается компактная топология для 4-битного сумматора с последовательным переносом на основе логики на проходных транзисторах. Полный сумматор моделируется при помощи инструментов автоматизированного проектирования, с получением временных диаграмм выходных сигналов демонстрирующих функциональность проектируемого устройства. Показано, что использование логики на проходных транзисторах при проектировании топологии 1-битного полного сумматора, состоящего из двух логических элементов XOR на трех транзисторах и одного мультиплексора на двух транзисторах, позволяет получить компактный 4-битный сумматор с последовательным переносом и обеспечить приемлемые характеристики выходных сигналов.

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